REMARKS/ARGUMENTS

Independent claim 1 recites a scheduler to receive via an instruction buffer and an instruction decoder at least two separate instruction groups, in a first stage map each of these groups to functional units independent of each other in which the scheduler treats each instruction group as having full access and availability to the multiple functional units, and in a second stage perform a merging and remapping of the instruction groups to at least part of the functional units to ensure that no resource conflict occurs. The cited art, including Hirata, fails to teach or suggest this subject matter. In this regard, scheduler unit 15 of Hirata does not perform these two stages of operation. Instead, in Hirata various operations are provided to instruction scheduler unit 15 from other front end units such as instruction set up units 14. Furthermore, there is not two separate mappings, namely a mapping and then a later merging and remapping of these groups. Instead, the instruction set up unit 14 provides instructions to instruction scheduler unit 15, which simply receives as inputs decoded instructions and distributes them to the functional execution units. This is not two separate stages, one of which is to map and a second of which is to merge and remap. Accordingly, claim 1 and the claims depending therefrom are patentable over the cited art. For at least similar reasons, independent claims 7 and 13 are similarly patentable.

The application is believed to be in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

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